

CIRCUIT DESCRIPTION

CD-94844-01
ISSUE 2B
APPENDIX 3A
DWG ISSUE 5A
DISTN CODE 1N99

16

COMMON SYSTEMS
PROGRAMMABLE SCANNER/DISTRIBUTOR
CIRCUIT

CHANGES

D. Description of Changes

- D.01 Correct erroneous wording of the option V.
- D.02 Provide a ground designation for external circuit use.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5251-BPE-RSP-GLW

CIRCUIT DESCRIPTION

CD-94844-01
ISSUE 2B
APPENDIX 2B
DWG ISSUE 4B
DISTN CODE 1N99

COMMON SYSTEMS
PROGRAMMABLE SCANNER/DISTRIBUTOR
CIRCUIT

CHANGES

B. Changes in Apparatus

B.01 Added

KS-16904,L2 Dust Covers

KS-16904,L5 Dust Covers

71A Connector Shield

B-138806-3 (Cinch Part No. DB59-20)
Dust Covers

D. Description of Changes

D.01 Add insulating sleeving on the INTB
terminal strip.

D.02 Modify wire gauges shown in FS3 and
CAD 7A and 7B.

D.03 Provide dust covers for the KS-16786,
L51, L54, and L55, KS-19087,L33 con-
nectors.

D.04 Equip all unmated 947-type connectors
with the 71A connector shield.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5251-BPE-RSP-GLW

CIRCUIT DESCRIPTION

CD-94844-01
ISSUE 2B
APPENDIX 1A
DWG ISSUE 3A
DISTN CODE 1N99

COMMON SYSTEMS
PROGRAMMABLE SCANNER/DISTRIBUTOR
CIRCUIT

CHANGES

D. Description of Changes

- D.1 Provide noise filter capacitors on RST0 and RSTB1 leads.
- D.2 Replace soldered connections of R1, R2, and R3 with wire wrapped connections.
- D.3 Provide access to the data bus control lead for the diagnostic and test unit.
- D.4 Eliminate local cable.
- D.5 Indicate -48V and RTN (ground) leads shown in FS3 shall be provided by the using circuit and connect to -48V and GRD. supply.

F. Changes in CD SECTION II

- F.1 In 9.06 change the first reference to "TBLAA and TBLBB" to read "TBLAA and TBLAB".
- F.2 In 10.04 change the reference to "TBLAA and TBLBB" to read "TBLAA and TBLAB".

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5251-AJI-BK-CB



COMMON SYSTEMS
PROGRAMMABLE SCANNER/DISTRIBUTOR
CIRCUIT

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SECTION I - GENERAL DESCRIPTION1. PURPOSE OF CIRCUIT

1.01 This circuit implements a general purpose unit which, through the use of a programmable control section, may be used in applications which require the observance and control of electromechanical circuits and the communication of information to an external device.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The circuit consists of a set of functional subunits which communicate with a Programmable Controller (PROCON) under the control of the PROCON. This communication takes place along a 16-bit bi-directional data bus. The PROCON which executes a unique, application oriented program, selects the source or destination of the information being transmitted on the bus by means of a 12-bit address bus and a 9-bit control bus.

2.02 The control bus contains four device select leads which function as an auxiliary address bus, three source leads which are used to gate information from one of the subunits onto the data bus, and two destination leads which clock information from the data bus into a register in one of the functional subunits. During a typical transfer of data, the PROCON will select a subunit by means of the 12-bit address bus and the four device select leads, then initiate the transfer of data by causing one of the source leads or one of the destination leads to be asserted. The leads of the control bus are buffered PROCON outputs, which are in turn under control of the instructions being executed in the PROCON.

2.03 The bidirectional data bus, during transfers of data from the PROCON to a functional subunit, is driven by the buffered PROCON output bus. During the transfer of data from a subunit to the PROCON, the data bus is disconnected from the output bus and is connected to the PROCON input bus, permitting the data bus to drive the PROCON input bus.

2.04 The address bus is driven by the buffered outputs of an address register, which is loaded with an address under control of the PROCON. The loading of this register takes place when the PROCON places data on its output bus and causes one of two control leads to be asserted. These control leads extend only from the PROCON to the address register, and are not part of the PSD control bus.

2.05 The PSD may be equipped with a 16-row by 16-bit Scanner Matrix - SD-94838-01. This circuit, when accessed, will place the data from a 16-bit row of scan points on the PSD data bus, from which it is transmitted to the PROCON. The row of scan points being accessed is selected by a row address present on the PSD address bus.

2.06 A 4-row by 16-bit Signal Distributor Matrix - SD-94839-01 may also be a part of the PSD. As in the case of the scanner matrix, a row of points is selected by the address present on the address bus. When this unit is accessed by the PROCON, the information on the PSD data bus will be latched into the appropriate row of signal distribute points.

2.07 The PSD may be optionally equipped with a combined Scanner Signal Distributor Matrix - SD-94851-01 in lieu of the separate scanner and signal distributor matrices previously described. This circuit, when accessed, will either place the data from a 10-bit row of scan points on the PSD data bus or latch the information from the PSD data bus into a 6-bit row of signal distribute points. The matrix is organized as a 16-row by 10-bit scanner and a 4-row by 6-bit distributor.

2.08 Random access storage is provided in the form of 2048 16-bit words of semiconductor memory. Information may be written into the memory from the data bus or read from the memory onto the data bus. The word of storage being accessed is determined by the address bus.

2.09 Accurate measurement of elapsed time is available to the PSD controller by means of a presetable interval timer. This timer is in the form of a 16-bit binary counter which, after being preset with information from the data bus, counts toward zero at the rate of one count for every cycle of the PROCON clock. Upon reaching a count of zero, the time will assert a time-out flag which may be read by the PROCON. This flag is reset when the timer is preset.

2.10 Transmission of information to and from the PSD proceeds via one or more (maximum of four) serial asynchronous data channels. Each channel is terminated by a data port in the PSD which communicates information with the PROCON (via the data bus) in parallel form while providing an EIA RS-232-C standard interface to the data channel. Each data port performs serial-to-parallel conversion on received data and parallel-to-serial conversion on transmitted data, while providing the proper formatting, checking, and timing of all transmitted and received data. Each data channel may operate at either 300 or 1200 baud, in either full duplex or half-duplex mode.

2.11 External manual control of the PSD operation is available through the use of four toggle switches, two momentary contact switches, and a pair of terminal strips to which external leads may be connected. The states of the toggle switches may, under control of the PROCON, be gated onto the PSD data bus and into the PROCON. The output of one of the momentary contact switches and five pins on the terminal strip are connected to PROCON test leads, and may be read directly. The remaining momentary contact switch causes a reset sequence to occur when it is depressed.

2.12 Indication of PSD operation status is provided by nine light emitting diodes and two mercury relay contact pairs. Seven of the light emitting diodes and one of the relays reflect the states of various bits in registers which may be loaded from the PSD data bus by an appropriate PROCON control sequence. The remaining light emitting diodes and relay are under the control of circuitry which monitors the PROCON operation and the state of the fuse alarm circuits. Correct operation of the PROCON is indicated by periodic (at intervals of less than 80 milliseconds) output operations which reset a sanity timer, and by an all-seems-well lead which reflects internal processor checks. A false all-seems-well indication or a sanity timer time-out will result in an automatic error indication.

SECTION II - DETAILED DESCRIPTION1. INTRODUCTION

1.01 This circuit consists of a programmable controller PROCON, a 16-row by 16-bit scanner matrix, a 4-row by 16-bit signal distributor matrix, or optionally a 16-row by 10-bit scanner matrix, 4-row by 6-bit signal distributor matrix combination, a random-access memory (RAM), asynchronous serial EIA data ports, and various timing and error detection circuits. Data is received, stored, and transmitted under the control of the PROCON, which executes a program stored in read-only memory (ROM).

2. DATA BUS

2.01 Data is transferred between the PROCON and the various functional subunits of the PSD via the 16-lead data bus. This bus is bidirectional, being driven by open collector gates in a WIRED-AND configuration. Pull-up resistors for each of the bus leads are provided on FC317 bus interface circuit packs.

2.02 During operations in which information is being sent from the PROCON to one of the subunits, the information on PROCON output bus leads $\overline{00B0}$ - $\overline{00B15}$ will drive PSD data bus leads DB000-DB150. The data bus drivers in this case are on the FC317 circuit pack, and are enabled by lead ENBO being at a low level. No inversion takes place between the PROCON output bus and the PSD data bus; on both buses, a low voltage (<0.4 volts) represents a logic 1.

2.03 Data may be gated onto the PROCON input bus (leads IBO-IB15) from one of three sources: the address register, the real-time clock, and the PSD data bus. Each source is connected to the input bus through open collector gates. When lead RDDB1 is at a high level, the PSD data bus will be gated onto the input bus, while a high level on lead RDAR1 gates the contents of the address register onto the input bus and a high level on lead RDRT1 will gate the contents of the clock onto the input bus. The three conditions are mutually exclusive; only one of the three gating leads will be high at any given time. Furthermore, the circuitry has been arranged such that lead RDDB1 remains at a high level.

2.04 When the PSD data bus is being gated to the input bus, lead ENBO will be driven to a high level. This prevents the data bus drivers on the FC317 from controlling the bus, and allows the bus to be driven by one of the functional subunits. In this way, data may be sent from a subunit to the PSD input bus.

2.05 The data on the PSD input bus is such that a logic 1 is represented by a lead at a high level (>2.4 volts). For this reason, a logic inversion exists between the input bus and the PSD data bus.

3. CONTROL BUS

3.01 The control leads from the PROCON are received by the FC318 circuit pack which, from them derives various clock and gating signals. In addition, these leads are buffered by the FC318 to drive the PSD control bus. In general, this buffering function is noninverting, with the state of a control bus lead following the state of the appropriate PROCON lead.

3.02 The PROCON source select leads, $\overline{0S0}$ and $\overline{0S1}$ drive control bus leads DI00 and DI10, respectively. These leads are normally at a high level, being driven low when asserted.

3.03 The device select leads from PROCON, NI0, NI1, NI2 and NI3, are buffered, respectively, to control bus leads DS01, DS11, DS21 and DS31.

3.04 Destination select leads $\overline{0D0}$ and $\overline{0D1}$ drive control bus leads D000 and D010 through gates which are enabled by a high level on the PROCON clock lead TCLK. Gating is such that a control bus lead will be driven low by a combination of a high level on lead TCLK and a low level on the appropriate destination select lead.

4. ADDRESS REGISTER

4.01 The 16-bit address register has been divided into two 8-bit bytes, each byte being on an FC317 bus interface circuit pack. The control signals necessary for writing and reading of the address register are received, decoded, then transmitted to the bus interface circuit packs by an FC318 interface controller circuit pack.

4.02 When writing into the address register, the PROCON will place the complement of the data on its output bus (00B0-00B15), then cause a low-going pulse on lead 0D2. This will in turn cause a high-going pulse on leads LDAR01 and LDAR11. The data on 00B0-00B15 is gated into the address register on the rising edge of these pulses and latched on the falling edge.

4.03 The outputs of the address register drive the leads of the PSD address bus (A000-A110) through open collector buffer circuits. There is no inversion from the PROCON output bus to the PSD address bus; a low-level signal on an output bus lead will result in a low-level signal on the corresponding address bus lead.

4.04 The lower byte of the address register may be written without affecting the upper byte. This is accomplished by a low-going pulse on lead 0D3, which results in a high-going pulse on lead LDAR01. Lead LDAR11 is not affected by this operation. The pulse on lead LDAR01 will cause the data on leads 00B0-00B7 to be latched into the low-order eight bits of the address register without affecting the high-order eight bits.

4.05 The contents of the address register are read by the PROCON during an operation in which the PROCON causes a low-going pulse on lead 0S2. This pulse will cause a high-going pulse on lead RDAR1 and a simultaneous low-going pulse on lead Rddb1. The high level on lead RDAR1 will cause the contents of the address register to be gated onto the PROCON input bus (leads IBO-IB15), while the low level on lead Rddb1 blocks the data path from the PSD data bus to the PROCON input bus.

4.06 A logic inversion exists in the address register data path, such that a low-level signal which has been latched into the address register from a lead of the PROCON output bus will appear as a high-level signal on the PROCON input bus when the address register is being read.

5. RANDOM ACCESS MEMORY

5.01 The PSD buffer storage is provided by one or more FB594 circuit packs, each of which contains 1024 words of semiconductor memory. Each word is capable of storing eight bits of data plus a parity bit. Individual words are addressed via the 12 leads of the PSD address bus (A000-A110), with leads A100 and A110 being used as a board select address. The state of A100 and A110 to which an individual FB594 will respond is determined by a set of PSD backplane straps. The low-order ten bits of the address bus define the memory word which is to be accessed on the selected board.

5.02 The PSD has been arranged such that 2048 words of 16 bits each are available. This has been accomplished by providing four FB594 circuit packs, one pair of which is selected by a high level on A100 and A110, the other pair being selected by a low level on A100 and a high level on A110. One board of each pair has been connected to the low order eight leads and the low-order parity bit (DB000-DB070, DBP00) of the PSD data bus, while the remaining board of each pair is wired to the high order eight leads and the high-order parity bit (DB080-DB150, DBP10) of the data bus.

5.03 Since addressing information is presented by the address bus in complemented form (negative logic) the lowest-order memory word is accessed when all leads of the bus are at a high level, while the highest-order word is addressed when A000-A100 are at a low level while A110 remains at a high level.

5.04 Data is written into a memory word by an operation in which the PROCON places the information on its output bus leads (00B0-00B15) while generating a low-going pulse on lead 0D0. This will cause a low-going pulse on lead D000 of the PSD control bus. Leads 00B0-00B15 are gated to the PSD data bus. As there is no inversion in the data path, the states of leads

DB000-DB150 should follow the states of leads 00B0-00B15 during this operation. Lead DBP00 transmits a parity bit which has been calculated over leads DB000-DB070. Parity is such that an even number of low-level leads results in a low level on DBP00. A similar calculation is performed on leads DB080-DB150 and presented on leads DBP10.

5.05 Upon receiving the low-going pulse on lead D000, the memory will store the data on leads DB000-DB150, DBP00 and DBP10 in the word specified by the address bus.

5.06 Information is read from the memory by an operation in which the PROCON generates a low-going pulse on lead 0S0. This results in a low-going pulse on lead DI00 which will cause the memory to place data from the addressed memory location on the PSD data bus. At this time, lead RDDBI will be at a high level, causing data present on the data bus to be inverted and gated onto the PROCON input bus. Thus an inverting data path is established from the memory to the PROCON input bus.

5.07 During memory read operations, parity is calculated over each byte of the data bus, inverted, and sent to a parity comparison circuit. This circuit receives, as inputs, DBP00, which is the low-order parity bit being read from memory, DBP10, which is the high-order parity bit being read from memory, and leads BPE11 and BPE01, which represent recalculated parity over the high and low bytes of the data bus. Correct data bus parity is indicated by DBP00 and BPE01 being in opposite states and DBP10 and BPE11 being in opposite states. This condition is checked at the falling edge of the signal on lead TCLK. If a mismatch has occurred, lead PTY is raised to a high level shortly after the falling edge on lead TCLK.

5.08 Address verification circuitry, resident on the FC318 circuit pack, further checks the validity of memory read or write operations. A falling edge on lead OS0 or ODO arms this checks circuitry, while a low level on lead AVO disarms it. If the check circuitry remains armed at the falling edge of the clock signal on lead TCLK, lead TO will be raised to a high level, indicating an error condition. (During a proper read or write of the memory, the appropriate FB594 circuit pack will pull lead AVO to a low level shortly after the reception of a falling edge on lead DI00 or lead D000.

5.09 Leads PTY and TO may be raised to a high level under the conditions described above. To bring these leads to a low level, it is necessary that the PROCON execute an instruction in which a low-going pulse is caused on lead OD1 while leads NI0 and NI3 are at a low level and leads NI1 and NI2 are at a high level.

6. SCANNER/DISTRIBUTOR

6.01 The PSD uses one or more Common Systems 4-Row X16-Bit Signal Distributor Matrix Circuit - SD-94839-01 and one or more Common Systems 16-Row X16-Bit Scanner Matrix Circuit - SD-94838-01 or one more 16-row by 10-bit scanner, 4-row by 6-bit Signal Distributor (Combined Scanner/Signal Distributor Matrix - SD-94851-01) for interface to electromechanical circuits. These distributor and scanner circuits are connected by a common inter-unit bus which is, in turn, connected to the PSD data, control, and address buses through an FC319 bus extender circuit pack. The FC319 provides termination and buffering for all bus leads and translates the PSD control bus signals into the control signals required by the scanner and distributor circuits.

6.02 Prior to a scan or distribute operation, the address register must be loaded with the address of the desired row. The leads of the PSD address bus, which are driven by the address register, are buffered, but not inverted by the FC319 and used to drive the address leads of the scanner/distributor interunit bus. Only the low-order eight leads of the PSD address bus are used, with PSD lead A000 driving scanner/distributor lead A1, PSD lead A010 driving scanner/distributor lead A2, etc. The address to which a row of scan or distribute points will respond is determined by a set of back-plane straps on the respective scan or distribute units. The proper strapping arrangement is defined in the appropriate SD.

6.03 A distribute operation will occur when the PROCON executes an instruction which causes complimented data to be put on its output bus (leads 00B0-00B15), leads NI0, NI1, and NI3 to be brought to a low level and lead NI2 to be brought to a high level while a low-going pulse is generated on lead OD1.

6.04 Data on the PROCON output bus will be buffered onto the leads of the PSD data bus (DB000-DB150). The FC319 circuit pack then buffers the PSD data bus to the scanner/distributor data bus (leads D0-D15). No inversion exists in the data path from the PROCON output bus to the scanner/distributor bus.

6.05 Leads N10, N11, N12 and N13 are buffered, but not inverted onto PSD control bus leads DS01, DS02, DS03 and DS04. The FS319, when seeing, respectively, low, low, high and low levels on these leads and a low-going pulse on lead D010, will generate required control signals to perform a distribute operation. Immediately following the low-going transition of lead D010, lead C1 will be brought low. Shortly thereafter, lead MSYN is brought low, remaining low for approximately 600 nanoseconds. Shortly after lead MSYN returns to a high level, lead C1 will be returned high. Information present on leads D0-D15 is entered into the selected row of distribute points about 400 nanoseconds after the falling edge of MSYN.

6.06 A scan operation is indicated by the PROCON generating a low-going pulse on lead OS1 while leads N10 and N11 are at a high level and leads N12 and N13 at a low level. Lead OS1 is buffered to lead DI10 of the control bus. During the time in which DI10 is at a low level and leads DS01, DS11, DS21, and DS31 are respectively high, high, low and low, the FC319 will cause MSYN to be pulled to a low level while lead C1 remains at a high level. At the same time, the scanner/distributor interunit bus will drive the PSD data bus.

6.07 When lead OS1 is at a low level, lead ENB0 will be driven high, disabling the data bus driving circuits on the FC317. Therefore, scan information present on the scanner/distributor bus will drive the PSD data bus which will, in turn, be inverted and presented to the PROCON input bus.

6.08 An address verify check, similar to that which takes place during memory read or write operations, is performed during scan or distribute operations. The checking circuit is armed by the low-going edge on lead OD1 on distributes or lead OS1 on scans, and disarmed by a low level on AV0. A low level on AV0 is generated by scanner/distributor bus lead SSYN being pulled low in response to a valid scan or distribute operation.

7. REAL-TIME CLOCK

7.01 A 16-bit binary counter has been provided with the PSD for use as a real-time clock. The counter has been divided into 8-bit segments, one of which is on each of the two FC317 circuit packs. The counter is presettable and readable, and counts at a rate determined by the frequency of the clock signal on lead TCLK.

7.02 During normal operation, the counter increments on the rising edge of a clock signal on lead RTCTL. This signal is normally identical to the signal on lead TCLK. Lead CTL1 ties the count-enable input of the low eight bits of the counter to a high level, permitting the lower eight bits to increment at every rising edge of lead RTCTL.

7.03 When the low-order eight bits of the counter reaches the all-ones state, an overflow condition is created. This results in lead CTH1 being raised to a high level for one clock cycle. Since CTH1 is tied to the count enable input of the high-order eight bits of the counter, the high-order portion of the counter will increment each time the low-order portion overflows.

7.04 An overflow of the counter (all 16 bits at a logic one) is indicated by a high level on leads CTH1 and OVST1. When lead OVST1 is at a high level, an overflow flag will be set on the falling edge of the signal on lead TCLK. The setting of the flag is indicated by lead T1 being driven to a high level.

7.05 Presetting of the counter is accomplished by causing a low-going pulse on lead OD1 while leads N10, N11, N12, and N13 are respectively low, high, low and low. Leads LDCL0 will be driven low and a short negative-going pulse will be generated on lead RTCTL. The rising edge of this pulse, occurring while lead LDCL0 is at a low level, will cause the information on leads 00B0-00B15 to be loaded into the counter. Additionally, if lead T1 is at a high level, it will be driven to a low level at the falling edge of the pulse on lead LDCL0.

7.06 The counter may be read into the PROCON by causing a low-going pulse on lead OS1 while leads N10, N11, N12, and N13 are respectively low, high, low and low. During the time in which lead OS1 is at a low level, lead RDRT1 will be driven high. This will permit the contents of the counter to be inverted and placed on the PROCON input bus.

8. I/O CHANNELS

8.01 The PSD is provided with a maximum of four EIA-compatible data ports. Each port is implemented on an FB595 or FB598 input output circuit. The FB595 data port contains three registers which are accessible to the PROCON. These include a received data register, from which input data may be read, a transmit data register, into which data to be sent over the data link is placed, and a readable status register, which indicates the operating mode of the data port. The FB598 data port contains the three registers for received data, transmitted data, and status, and an additional writable register which controls the transmitted data format.

8.02 Data is written to the transmit data register of a given FB595 or FB598 circuit pack by an operation in which the data is placed on the low eight bits of the PROCON output bus and a low-going pulse is generated on lead ODI while lead NI0 is at a high level. The states of leads NI1, NI2 and NI3 determine which of the individual data ports are accessed. The levels to which a given board will respond are determined by a set of PSD backplane straps.

8.03 Data which has been entered into the transmit register will be transmitted serially from the data port on lead BA. (The actual lead name depends on the data port number. For example, data port 0 transmits on lead OBA.) The detailed format of data transmission is determined by a select switch on the FB595, or the FB598 control register but in general, each transmitted character consists of a start bit (+9 volts), the proper data bits, and one or two stop bits (-9 volt level). A data bit which is entered into the transmit register from a low-level lead of the PSD data bus, (ie, a logic 1) will appear as a -9 volt signal on lead BA. Order of transmission is such that the low-order bit of the data word immediately follows the start bit. Data is transmitted at either 300 baud or 1200 baud, depending on the state of a select switch on the FB595 circuit pack or a backplane strap for the FB598 circuit pack. When no data is being transmitted, lead BA remains at -9 volts.

8.04 Serial information is received by the data port on lead BB. This data, which is of the same format as that being transmitted, is converted from serial to parallel form and placed in the received data register by the data port. The contents of this register are gated onto the PSD data bus by the data port when a low-going pulse is generated on lead OSI while lead NI0 is at a high level. As mentioned above, the required levels of leads NI1, NI2, and NI3 are determined by backplane straps.

8.05 Format checking of received data is performed by the FB595 or FB598. The result of this checking is available in the data port status register; the contents of this register are gated to the PSD data bus by an operation in which OSI is pulsed low while lead NI0 is at a low level. Again, the levels on leads NI1, NI2, and NI3 determine which data port is being accessed. The status register also contains bits which indicate whether or not a character may be read from the received data register and whether or not a new character may be loaded into the transmit data register.

8.06 An LED indicating the state of lead CF (carrier detect) is mounted on each FB595 circuit pack. The LED will be off when lead CF is at +9 volts, and turned on when the lead is at -9 volts or floating.

8.07 A toggle switch is mounted on the edge of each FB595 such that it may be operated while the circuit is inserted in the PSD. The switch has no control over the operation of the data port, but the bits state is read as a bit in the data port status register. (The switch is typically used as an out of service indicator.) The state of the FB595 carrier-detect LED is also available as a status register bit.

8.08 Each FB595 data port has driving circuitry to maintain leads CA and CD at a level of +9 volts to +12 volts.

8.09 Leads _CB and _CC control the transmission and reception of serial data for the FB595 circuit pack. If either or both of these leads is driven to -9 volts, data on lead _BB will not be recognized and no data will be transmitted on lead _BA. When both leads are at +9 volts, the data port operates normally.

8.10 Leads _CA, _CD, and _SCA are controlled by the writable control register of the FB598 circuit pack. This register, which also controls the transmitted data format, may be written with data on the low eight bits of the PROCON output bus by generating a low-going pulse on lead OD1 while lead NIO is at a low level.

8.11 Leads _SCA, _SCF, _CC, _CB, _CE, _CF, _CD, and _CA may be read from the FB598 circuit pack. The EIA status register contents are gated to the PSD data bus by an operation in which lead OS2 is pulsed low while lead NIO is at a low level. The levels on leads NI1, NI2, and NI3 determine which data port is being accessed.

9. CONTROL AND TROUBLE INDICATION

9.01 Indication and control of the operational state of the PSD is provided by means of several switches, light-emitting diodes and mercury-relay contact pairs. Interfacing these switches, LEDs and relays to the electronic portion of the PSD is the function of the FB596 regulator/relay circuit pack and the FB597 trouble indication circuit pack.

9.02 The state of the CONTROL 1, CONTROL 2, CONTROL 3, and CONTROL 4 toggle switches are presented to the FB597 circuit pack on leads TC01, TC11, TC21, and TC31. A switch in the raised position will allow the appropriate lead to be pulled to a high level by a resistor on the FB597. A switch in the down position will ground the associated lead.

9.03 An operation in which the PROCON causes a low going pulse on lead OS1 while leads NI0, NI1, NI2, and NI3 are all at a low level will result in the state of leads TC01, TC11, TC21, and TC31 being inverted and gated onto the low-order four leads of the PSD data bus (D000-D030). At the same time, the data bus leads will be gated to the PROCON input bus.

9.04 The four light-emitting diodes which have been labeled CONTROL 1, CONTROL 2, CONTROL 3, and CONTROL 4 are driven by the buffered outputs of a 4-bit latch on the FB597 circuit pack. This latch is loaded from the four low order leads of the PSD data bus during an operation in which a low going pulse is generated on lead OD1 while leads NI0, NI1, NI2, and NI3 are all at a low level. A LED will be turned on by its associated latch bit being loaded from a low level data bus lead. Each LED is driven by an open collector buffer and is wired in series with a current limiting resistor on the FB597 circuit pack.

9.05 A similar situation exists for the LEDs labeled SD, MEM, and I0. However, the latch which drives these LEDs is loaded by an operation in which lead OD1 is pulsed low while leads NI0 is at a high level, and leads NI1, NI2, and NI3 are all at a low level. These LEDs reflect the states of the latch bits which are loaded from data bus leads DB000, DB010 and DB020, respectively.

9.06 An additional two latch bits, connected to bits DB030 and DB040 of the data bus, will be loaded during the above operation. A low level on the appropriate data bus lead results in lead AE0 or BE0, respectively, being latched at a low level which, in turn, results in the operation of mercury contact relays on the FB596 circuit pack. Lead AE0 being pulled low will cause a contact pair closure which establishes continuity between leads TBLAA and TBLBB; a low level on lead BE0 will cause continuity to be established between leads TBLBA and TBLBB.

9.07 A sixth latch bit is also loaded during this operation. This latch bit, however, is located on the FC318 circuit pack. It is loaded from lead 00B5, and its state is reflected by the level of lead CA0. A low level being latched from lead 00B5 will result in lead CA0 being pulled low. This, in turn, will cause lead AE0 to be pulled low and, additionally, will cause the CONT LED to be lit.

9.08 The states of these six latch bits may be gated onto the PSD data bus by a low-going pulse on lead OSI while lead NI0 is at a high level and leads NI1, NI2 and NI3 are all at a low level. A latch bit which has been set such that the associated LED or relay is operated which cause the appropriate data bus lead to be pulled low. The data bus leads are, at the same time, inverted and gated onto the PROCON input bus.

9.09 The TEST pushbutton on the control panel functions as a lamp test switch. When the switch is depressed, lead LT0 will be pulled to a low level, causing all above-mentioned LEDs to be operated.

9.10 The control panel switch labeled EX is tied directly to lead T3. This lead will remain at a low level except when the switch is depressed. During that time, the lead will be pulled to a high level by a pull-up resistor on an FC317 circuit pack.

9.11 The momentary contact INIT switch, when depressed, will cause lead RST0 to be pulled to a low level while lead RST1 is pulled high. These transitions will cause a low going pulse on lead RESET. This pulse will be of approximately 30 micro-seconds duration. Releasing the INIT switch will cause lead RST0 to return to a high level and lead RST1 to return low.

9.12 Two hardware checks of PROCON sanity are included on the FC318 circuit pack. The first of these is a sanity timer, which must be reset at an interval of less than 80 milliseconds. This resetting is accomplished by an operation in which the PROCON causes a low going pulse on lead OD1 while leads NI0 and NI1 are at a high level and leads NI2 and NI3 are at a low level. If the timer is allowed to time out, the latch bit associated with the CONT LED will be set. This will be indicated by lead CA0 being driven to a low level and the CONT LED being lighted.

9.13 The second hardware check of the PROCON involves monitoring of lead ASW. If this lead is at a low level during the falling edge of the clock signal on lead TCLK, lead CA0 will be driven low in the same manner as if a sanity timer time out had occurred. This check is inhibited during the first negative transition on lead TCLK following a system initialization.

9.14 Five leads have been provided which may be grounded or allowed to float to +5 volts under the control of external circuitry. These leads, named T2, T4, T5, T6, and T7, are available on terminal strip INTB.

10. POWER AND FUSING

10.01 The PSD obtains power from standard -48 volt nonfiltered office battery. A 132H dc-dc power converter transforms the office battery into the five volts required the logic circuitry and ± 16 volts required by the FB595 and FB598 circuit packs. The ± 16 volts is low current and poorly regulated, and must be further conditioned by series regulators on the FB596 regulator/relay circuit pack. The output of the FB596 is ± 12 volts, which is tied directly to the FB595 or FB598 circuit packs via leads P12V and M12V.

10.02 All voltage supply leads are fused. The input office battery is tied to the scan units through fuse SPB and to the 132H power converter through fuse PF. The 5-volt output of the power converter is connected to the PROCON and to the control panel through fuses C0 and CD0, respectively. Power at +5 volts is applied to the scanner and distributor through fuse SD0, while fuse REF supplies +5 as a reference voltage to the regulators on the FB596. Fuses PD0 and PD1 supply current at +5 volts to the remainder of the logic circuitry. Fuses I0P and I0M supply +16 volts and -16 volts from the 132H converter to the FB596 circuit pack.

10.03 The 132H converter, when properly installed, is operated by the PWR switch on the control panel. When this switch is down -48 volts will be applied to the remote start lead of the converter, keeping it off. However, when the PWR switch is raised to the ON position, this lead is allowed to float and the converter will operate.

10.04 The failure of a fuse supplying a positive voltage (+5 or +12) will result in lead FAP being raised to approximately +5 volts, while the failure of a negative-voltage fuse (-48 volts or -12 volts) will cause approximately -5 volts to be applied to lead FAM. Either (or both) of these conditions will operate the fuse alarm relay on the FB596 circuit pack which will, in turn, cause a contact closure establishing continuity between leads TBLAA and TBLBB. At the same time, the FA LED will be lighted by a voltage applied to it via leads FALC and FALA.

10.05 The FA LED will also be lit when the TEST button is depressed. In this instance, lead FALT will be driven to +5 volts. This condition will cause a positive voltage to be developed between leads FALC and FALA but will not operate the fuse alarm relay.

10.06 Failures in the 132H converter are indicated by the lighting of an LED on the converter and by the closure of an alarm relay within the converter. This closure is indicated by the establishment of continuity between leads TBLAA and TBLAB.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltage Limits

<u>Voltage</u>	<u>Min</u>	<u>Max</u>
-48V	-55V	-42.5V

1.02 TEMPERATURE LIMITS

Operating temperature range is 0° to 50°C ambient.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packages

<u>Designation</u>	<u>Meaning</u>
BEX	Bus Extender
BI0,BI1	Bus Interface 0 and 1
ICNT	Interface Controller
IØ0-3	Input/Output Port 0 through 3
RAM0-3	Random Access Memory 0 through 3
RGRL	Regulator/Relay
TBI	Trouble Indication

2.02 Signal Leads

<u>Designation</u>	<u>Meaning</u>
AEO	A Relay Enable
ASW	PROCON All-Seems-Well
AVO	Address Verify
A000- A110	Address Bus Leads 0 through 11
A1-A8	Scanner/Distributor Address Leads 1 through 8
BEO	B Relay Enable
BPE01, BPE11	Bus Parity Even 0 and 1
CAO	Controller Alarm
CI	PROCON Clock Inhibit
CTL1	Low-Order Count Enable
CTH1	High-Order Count Enable
CTLO	CONT LED Enable
Cl	Scanner/Distributor Control Lead

<u>Designation (Cont)</u>	<u>Meaning</u>	<u>Designation (Cont)</u>	<u>Meaning</u>
DBP00, DBP10	Data Bus Parity 0 and 1	RDAR1	Read Address Register
DB000- DB150	Data Bus Leads 0 through 15	Rddb1	Read Data Bus
DI00- DI20	Data In 0 through 2	RDRT1	Read Real-Time Clock
D000, D010	Data Out 0 and 1	RESET	Master Reset
DS01- DS31	Device Select 0 through 3	RSTAL	Reset Lead A
D0- D15	Scanner/Distributor Data Leads 0 through 15	RSTO	Reset
ENB0	Enable Data Bus	RTCT1	Real-Time Clock Count
FALA	FA LED Anode	SDEO	SD LED Enable
FALC	FA LED Cathode	SSYN	Scanner/Distributor Slave Sync
FALT	FA LED Test	TBLAA, TBLAB	A Relay Contacts A and B
FAP	Fuse Alarm Plus	TBLBA, TBLBB	B Relay Contacts A and B
FAM	Fuse Alarm Minus	TCLK	Clock
IB0- IB15	PROCON Input Bus 0 through 15	TC01- TC31	CONTROL Switch Leads 0 through 3
I0E0	I/0 LED Enable	T00- T30	CONTROL LED Enables 0 through 3
LDAR01, LDAR11	Load Address Register 0 and 1	T0-T7	PROCON TEST LEADS 0 through 7
LDCL0	Load Clock	OBA- 3BA	Transmitted Data (EIA) 0 through 3
LT0	Lamp Test	0BB- 3BB	Received Data (EIA) 0 through 3
MEMO	MEM LED Enable	0CA- 3CA	Request-to-Send (EIA) 0 through 3
MSYN	Scanner/Distributor Master Sync	0CB- 3CB	Clear to Send (EIA) 0 through 3
NI0- NI3	PROCON Device Select Leads 0 through 3	0CC- 3CC	Data Set Ready (EIA) 0 through 3
OVST1	Clock Overflow	0CD- 3CD	Data Terminal Ready (EIA) 0 through 3
PTY	PROCON Parity Lead		

<u>Designation (Cont)</u>	<u>Meaning</u>
OCF- 3CF	Received Line Signal Detector (EIA) 0 through 3
OD0- OD3	PROCON Destination Select Leads 0 through 3
00B0- 00B15	PROCON Output Bus 0 through 15
OSCA- 3SCA	Secondary Request-to-Send (EIA) 0 through 3
OSCF- 3SCF	Secondary Received Line Signal Detector (EIA) 0 through 3
OCE- 3CE	Ring Indicator (EIA) 0 through 3
OS0- OS2	PROCON Source Select Leads 0 through 2

2.03 Connectors

<u>Designation</u>	<u>Meaning</u>
OUT	Scanner/Distributor Bus Output
I/00- I/03	Data Channel Connectors 0 through 3

2.04 Terminal Strips

<u>Designation</u>	<u>Meaning</u>
INTA	Office Interface A
INTB	Office Interface B
PWR	Power

3. FUNCTIONS

- 3.01 Provide access to electromechanical office-equipment via a matrix of scan and distribute points.
- 3.02 Provide temporary storage of information.
- 3.03 Provide data channels for interchange of information with remote locations.

3.04 Provide a means of accurate event timing.

3.05 Control the above circuitry with a programmable controller (PROCON) such that the detailed functioning of the equipment depends on the program within the controller.

3.06 Provide control and error checking of the PROCON operation.

4. CONNECTING CIRCUITS

4.01 None.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing test requirements are specified in the X-79008 specification.

SECTION IV - REASONS FOR REISSUEB. Changes in ApparatusB.1 Added

I00-3 - FB598 Circuit Pack -
Option Y, FS1 - App Fig. 3

D. Description of Changes

D.01 The FS1 has been revised to show the addition of option W. Wiring not formerly designated has been designated option X.

D.02 The FS1 has been revised to show the addition of option Y. Circuit pack code and wiring not formerly designated have been designated option Z.

D.03 The FS1 has been revised to show option N. This wiring was previously provided on a nonoption basis.

D.04 The FS1 has been revised to show the addition of options Q, R, S, and T.

D.05 The FS2 has been revised to show the addition of option V.

D.06 The FS2 has been revised to show the 1C contact of the INIT switch removed from the CDO fuse and connected to ground.

- D.07 Apparatus Fig. 1 has been changed to show the addition of option W as noted in D.01.
- D.08 Apparatus Fig. 2 has been modified to show reference to Information Note 307.
- D.09 Apparatus Fig. 3 has been revised to reflect changes noted in D.02.
- D.10 Circuit Note 101 has been modified and Note 102 has been replaced by Notes 102A and 102B.
- D.11 Equipment Notes 205 and 206 have been added.
- D.12 Information Notes 306, 307 and 308 have been added.
- D.13 Cross Connection Note 403 has been added.
- D.14 The CAD 1 has been revised to reflect the changes noted in D.02.
- D.15 The CADs 2, 3, 4, and 5 have been rated Mfr Disc. and replaced by CADs 15, 16, 17, and 18 respectively.
- D.16 The CAD 6 has been modified to reflect changes noted in D.06 and to show frame or switchboard cable where local cable was formerly specified.
- D.17 The CADs 7A and 7B have been revised to reflect changes noted in D.01.
- D.18 The CAD 8 has been changed to show local cable and to show solder sleeve assemblies per the new Equipment Note 205 referred to in D.11.
- D.19 The CADs 9 and 11 have been rated Mfr Disc. and replaced by CADs 13 and 14 respectively.
- D.20 The CAD 12 has been revised to reflect changes noted in D.19.

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